Digital Blackbox Solution

IEEE at WashU Fall 2024

Washington University in St. Louis

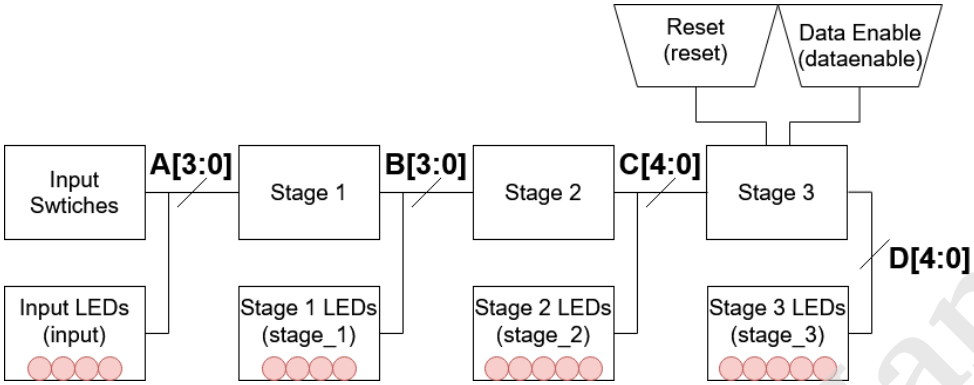

Figure 0.1: Block diagram of the digital system

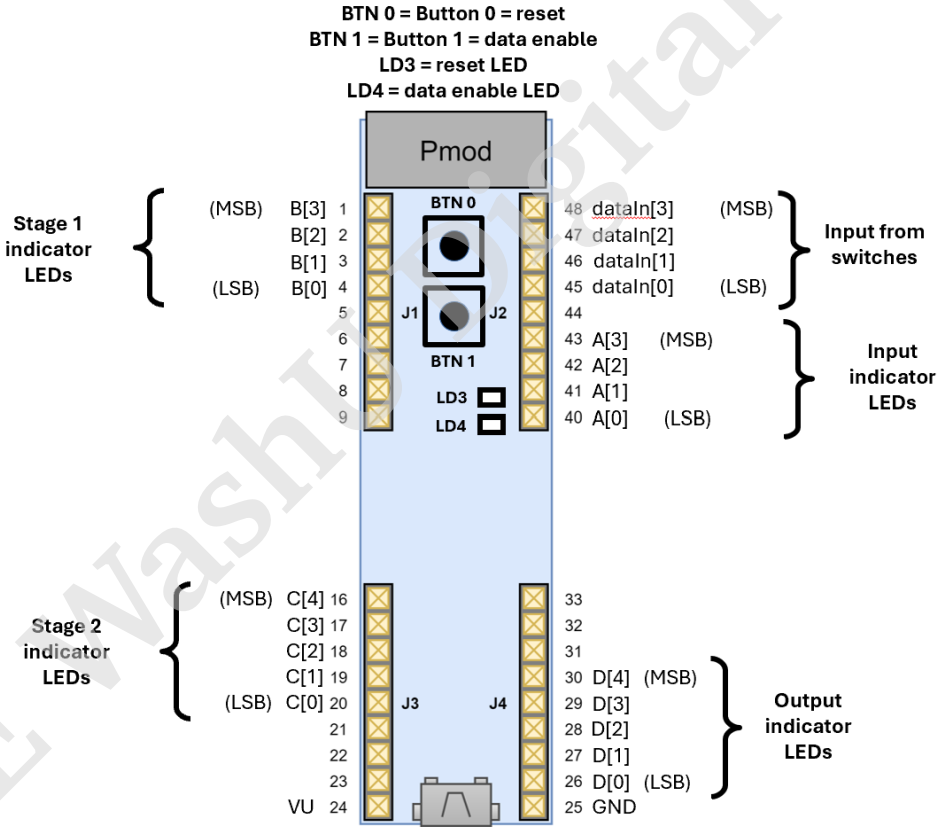

Figure 0.2: Pin-out of the CMOD S7 for all input and outputs

Input Switches will be labeled: A_3 through A_0, outputs of stage 1 labeled: B_3 through B_0, outputs of stage 2 labeled: C_4 through C_0, and the final output labeled as D_4 through D_0.

IEEE WashU Digital Handout

0.1 Point Assignment

Table 0.1: Point Distribution

Stage	Category	Points	Total
Stage 1:	Correct Truth Table Values	1	64
	Simplified Boolean Equations (SoP)	5	20
	Simplified Logic Diagram		16
	Detecting Functionality		20
		Total	**115**
Stage 2:	Correct Truth Table Value	1	80
	Every simplified Equation (SoP)	5	25
	Simplified Logic Diagram		20
		Total	**145**
Stage 3:	Detecting Functionality		40
		Total	**40**
		TOTAL SUM:	**300**

IEEE WashU Digital Solution

1 Stage 1

Inputs into the stage are $[A_3, A_0]$ and the outputs are $[B_3, B_0]$.

Table 1.1: Truth Table for stage 1 with inputs A[3:0] and outputs B[3:0]

A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
0	0	0	0	1	0	0	0
0	0	0	1	1	0	0	1
0	0	1	0	1	0	1	1
0	0	1	1	1	0	1	0
0	1	0	0	1	1	1	0
0	1	0	1	1	1	1	1
0	1	1	0	1	1	0	1
0	1	1	1	1	1	0	0
1	0	0	0	0	1	0	0
1	0	0	1	0	1	0	1
1	0	1	0	0	1	1	1
1	0	1	1	0	1	1	0
1	1	0	0	0	0	1	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	0	1
1	1	1	1	0	0	0	0

IEEE WashU Digital Solution

Table 1.2: Kernal map for B_3

$A_3A_2 \backslash A_1A_0$	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	0	0	0	0
10	0	0	0	0

Table 1.3: Kernal map for B_2

$A_3A_2 \backslash A_1A_0$	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

Table 1.4: Kernal map for B_1

$A_3A_2 \backslash A_1A_0$	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	0
10	0	0	1	1

Table 1.5: Kernal map for B_0

$A_3A_2 \backslash A_1A_0$	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

For B_3 from table 1.2: $B_3 = \overline{A_3}$
For B_2 from table 1.3: $B_2 = \overline{A_3}A_2 + A_3\overline{A_2} = A_3 \oplus A_2$
For B_1 from table 1.4: $B_1 = A_2\overline{A_1} + \overline{A_2}A_1 = A_2 \oplus A_1$
For B_0 from table 1.5: $B_0 = \overline{A_1}A_0 + A_1\overline{A_0} = A_1 \oplus A_0$

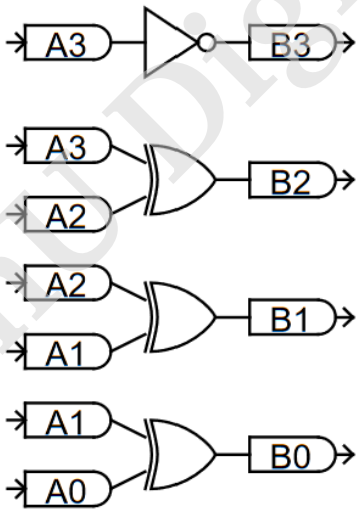

Figure 1.1: Circuit Diagram of Stage 1

IEEE WashU Digital Solution

2 Stage 2

Table 2.1: Truth Table for stage 2 with inputs A[3:0] and outputs B[3:0]

B_3	B_2	B_1	B_0	C_4	C_3	C_2	C_1	C_0
0	0	0	0	1	0	1	1	1
0	0	0	1	1	0	1	0	1
0	0	1	0	0	0	1	0	1
0	0	1	1	0	1	1	0	1
0	1	0	0	1	0	0	1	1
0	1	0	1	1	1	0	1	0
0	1	1	0	0	0	0	0	1
0	1	1	1	0	1	1	1	1
1	0	0	0	0	0	1	1	0
1	0	0	1	0	0	1	0	0
1	0	1	0	1	0	1	1	0
1	0	1	1	1	1	1	0	1
1	1	0	0	0	1	0	0	0
1	1	0	1	0	1	0	1	0
1	1	1	0	1	1	0	0	0
1	1	1	1	1	1	0	1	1

Table 2.2: Kernal map for C_4

$B_3B_2 \backslash B_1B_0$	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	0	0	1	1
10	0	0	1	1

Table 2.3: Kernal map for C_3

$B_3B_2 \backslash B_1B_0$	00	01	11	10
00	0	0	1	0
01	0	1	1	0
11	1	1	1	1
10	0	0	1	0

Table 2.4: Kernal map for C_2

$B_3B_2 \backslash B_1B_0$	00	01	11	10
00	1	1	1	1
01	0	0	1	0
11	0	0	0	0
10	1	1	1	1

Table 2.5: Kernal map for C_1

$B_3B_2 \backslash B_1B_0$	00	01	11	10
00	1	0	0	0
01	1	1	1	0
11	0	1	1	0
10	1	0	0	1

Table 2.6: Kernal map for C_0

$B_3B_2 \backslash B_1B_0$	00	01	11	10
00	1	1	1	1
01	1	0	1	1
11	0	0	1	0
10	0	0	1	0

IEEE WashU Digital Solution

For C_4 from table 2.2: $C_4 = \overline{B_3}\,\overline{B_1} + B_3B_1$
For C_3 from table 2.3: $C_3 = B_3B_2 + B_2B_0 + B_1B_0$
For C_2 from table 2.4: $C_2 = \overline{B_2} + \overline{B_3}B_1B_0$
For C_1 from table 2.5: $C_1 = B_2B_0 + B_3\overline{B_2}\,\overline{B_0} + \overline{B_3}\,\overline{B_1}\,\overline{B_0}$
For C_0 from table 2.6: $C_0 = \overline{B_3}\,\overline{B_2} + B_1B_0 + \overline{B_3}\,\overline{B_0}$

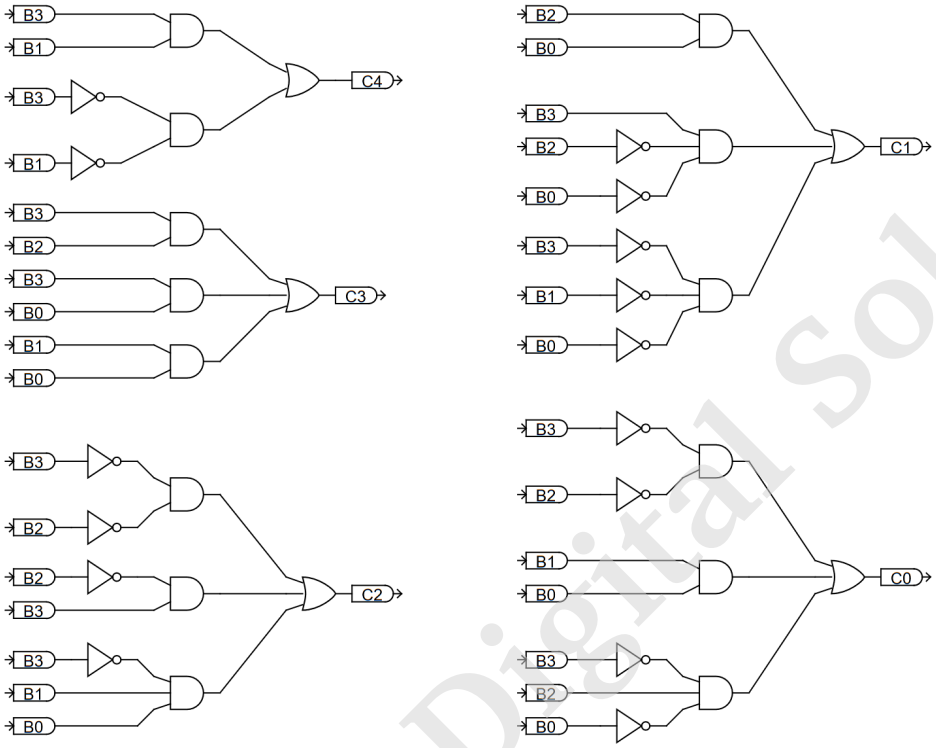

Figure 2.1: Stage 2 Circuit Diagram

IEEE WashU Digital Solution

3 Stage 3

Stage 3 is an ALU, where C[4] controls whether it is doing addition $C_4 == 0$ or subtraction $C_4 == 1$ and C[3:0] is the primary input of the ALU and the output of the ALU is fed to the LED outputs as well as a register triggered by the contestants, which goes into the secondary ALU input. The diagram can be found in fig. 3.1.

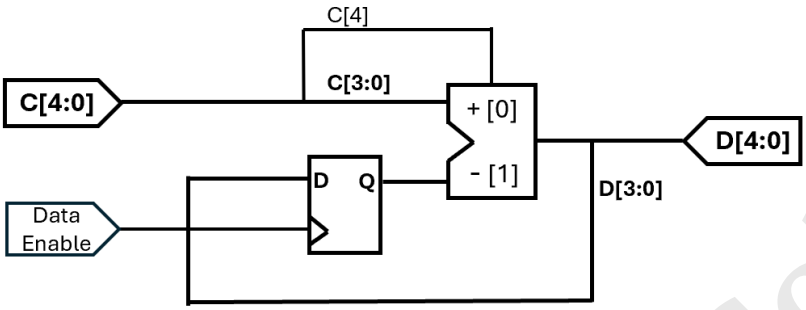

Figure 3.1: Stage 3 Diagram

IEEE WashU Digital Solution